VDU-A

Function.

This board is used to generate the line and frame synchronisation pulses for the video signal together with additional pulses to control the widths of the left-hand and upper margins of the display. All these signals are derived from a single master oscillator so that all the sigrals are synchronised with one another. A 1 MHz signal is also available for use as a clock for a microprocessor.

Operation.

IC1 is used with a 7 MHz quartz crystal as the master oscillator. A buffered 7 MHz output is provided at the edge connector. IC2 & 3 form a divide by seven circuit to produce 1 MHz. This is then further divided by 64 using LC4 & 5 to give the line frequency of 15.625 KHz and by 625 using IC8,9,10 & 11 to the frame rate of 50Hz. Signals from IC4 & 5 are taken to a decoder (IC6) to provide a series of 2μS wide pulses at the outputs of IC6. A 6μS wide negative going pulse for the line sync. (LS) is generated by setting a bistable ($\frac{1}{2}$ of IC7) from the line frequency and resetting it with output 3 from the decoder. Similarly the line sync delay pulse (LSD) is produced using the other half of IC7 as a bistable, which is set by LS and reset by an output from IC6. The output can be selected to give pulse widths from 2μS to 12μS using J1. This determines the width of the left-hand margin. LSD is positive going and overlaps LS.

A frame sync. signal (FS) of $7\frac{1}{2}$ lines width and negative going, is produced by delaying FS with IC12a and gating this with the original signal. An adjustable FSD signal is generated using circuitry similar to that for LSD, except that the bistable (IC12b) is set by the trailing edge of FS, so that FS and FSD do not overlap. The width of FSD is selected using J2 and determines the width of the upper margin. Since FS is derived by dividing the twice-line frequency by an odd number, the LS pulses alternate between starting exactly with FS, and starting with a half line delay. This produces the correct pulse relationships for an interlaced display.

JSD 5.12.78

Drn. TSD

Date 5/12/78

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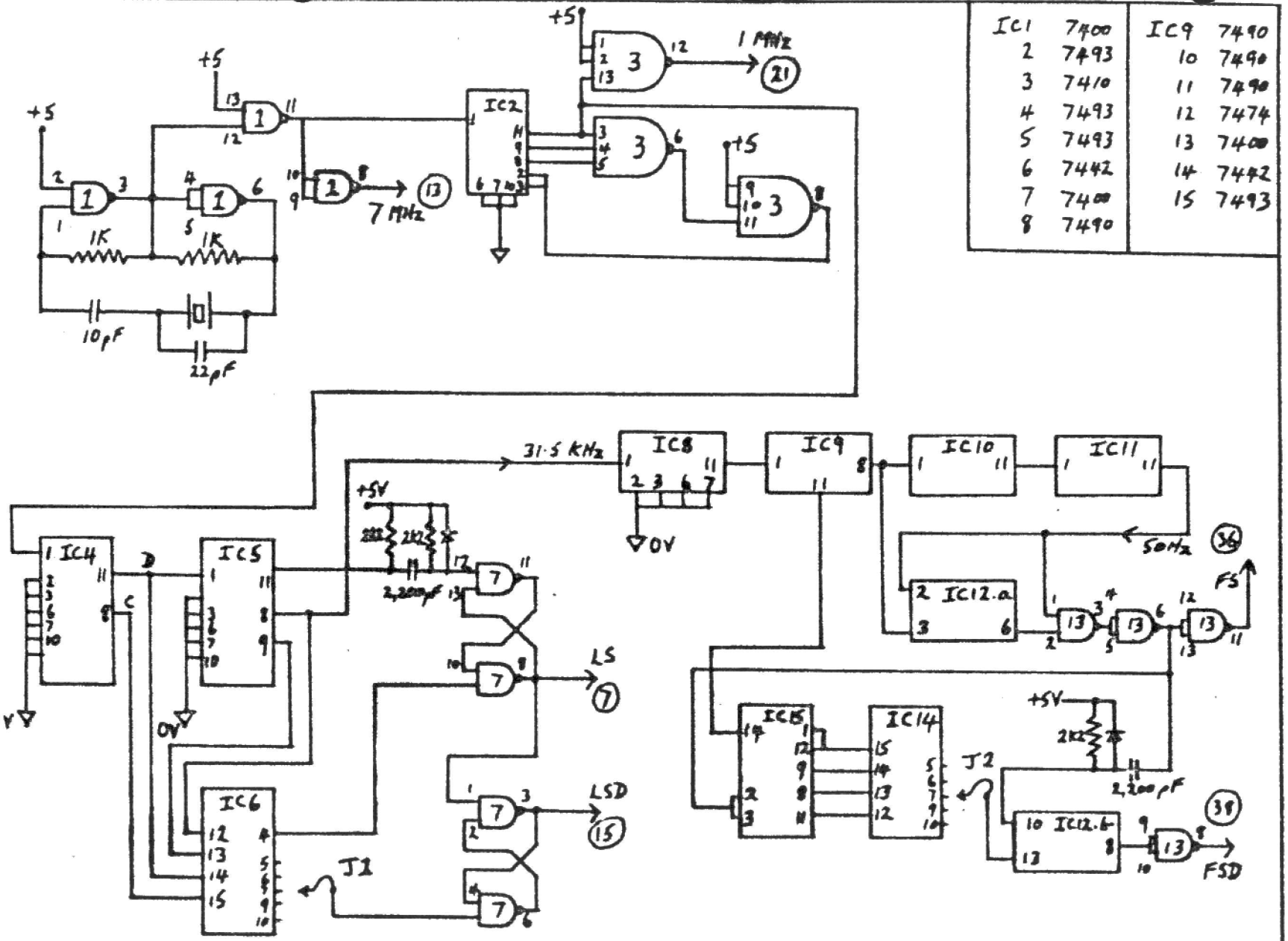
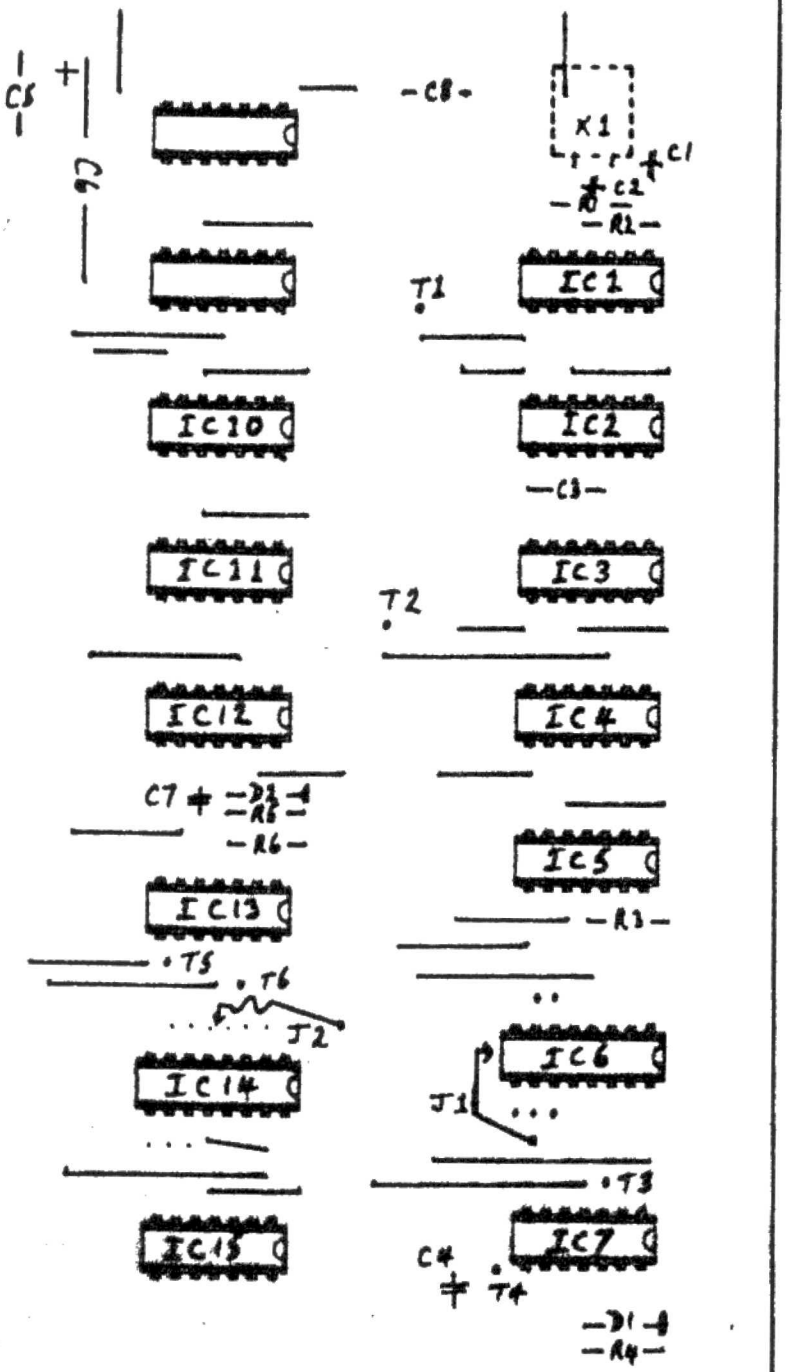
VDU·A·2



IC1	7400	IC9	7490
2	7493	10	7490
3	7410	11	7490
4	7493	12	7474
5	7493	13	7400
6	7442	14	7442
7	7400	15	7493
8	7490		

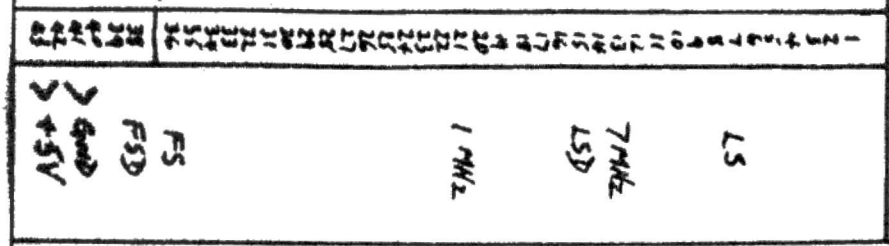


COMPONENTS

R1	1k	(4k7)
2	1K	(4k7)
3	2k2	(10k)
4	2k2	(4k7)
5	2K2	(4k7)
6	2K2	(10k)
C1	10pF	
(2	22pF)	
3	0·1μ	DISC
4	2,200pF	(1,000pF)
5	0·1μ	DISC
6	100μ	10V
7	2,200pF	(1,000pF)
8	0·1μ	DISC
D1	IN914	
2	IN914	
X1	7MHz	CRYSTAL
IC1	7400	
2	7493	
3	7410	
4	7493	'LS SERIES
5	7493	DEVICES CAN
6	7442	BE USED
7	7400	INSTEAD,
8	7490	AND CHANGE
9	7490	RT VALUES
10	7490	IN BRACKETS
11	7490	
12	7474	
13	7400	
14	7442	
15	7493	

TEST POINTS: —

T1	7MHz
2	1MHz
3	LSD
4	LS
5	FSD
6	FS



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Drn. BSD	Date 5/12/78

VDU·A·2